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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
PIZIALI, J	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/653,583	MIKAMI ET AL.	
	Examiner	Art Unit	
	Jeff Piziali	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/820,835* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copies have been filed in parent Application No. 08/820,835, filed on March 19, 1997.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-17 are rejected under the judicially created doctrine of double patenting over claims 1-24 of U. S. Patent No. 6,115,017 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: a liquid crystal display apparatus having a pair of substrates of which at least one substrate is transparent and a liquid crystal layer sandwiched between the substrates, comprising

a plurality of scanning electrodes formed on one of the substrates; and a plurality of signal electrodes intersecting in a matrix form with the plurality of scanning electrodes; wherein the display apparatus further comprises, within each of the regions surrounded by the plurality of scanning electrodes and the plurality of signal electrodes: a display data holding circuit connected to a corresponding scanning electrode and signal electrode, for fetching and storing display data from a signal electrode in response to a scanning signal for holding a display image without updating the display data while a power supply to the display apparatus is maintained; a switching device connected to the display data holding circuit, its switching operation being controlled by the display data holding circuit; and a display electrode connected to the switching device.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 5-10 and 12-17 rejected under 35 U.S.C. 102(b) as being anticipated by Hamada et al. (5,194,974).

In regards to claim 1, Hamada et al. disclose a liquid crystal display apparatus having a pair of substrates of which at least one substrate is transparent (see Column 6, Line 15) and a liquid crystal layer sandwiched between the substrates (see Column 1, Lines 20-21), comprising:

a plurality of scanning electrodes formed on one of the substrates (see Figure 2 and Column 5, Line 55); and

a plurality of signal electrodes intersecting in a matrix form with the plurality of scanning electrodes (see Figure 2 and Column 5, Line 54);

wherein the display apparatus further comprises, within each of the regions surrounded by the plurality of scanning electrodes and the plurality of signal electrodes:

(a) a display data holding circuit (TFT1 and C1) connected to a corresponding scanning electrode and signal electrode, for fetching and storing display data from a signal electrode in response to a scanning signal (see Figure 4 and Column 6, Lines 54-55) for holding a display image (in C1) without updating the display data (in C2) while a power supply (Vc) to the display apparatus is maintained (see Figure 1; Column 6, Lines 59-65);

(b) a switching device (TFT2) connected to the display data holding circuit, its switching operation being controlled by the display data holding circuit (see Figure 4 and Column 6, Lines 59-65); and

(c) a display electrode (C2) connected to the switching device (see Figure 4 and Column 5, Lines 66-68).

In regards to claim 2, Hamada et al. disclose that an opposed electrode which faces the display electrode is provided on the other substrate of the pair of substrates, and a common electrode connected to a switching device within each of the regions is provided on one substrate thereof (see Figure 4 and Column 8, Lines 33-38).

In regards to claim 5, Hamada et al. disclose a display data holding circuit (TFT1 and C1) connected to a common electrode (C2) (see Figure 1; Column 5, Lines 53-65).

In regards to claim 6, Hamada et al. disclose a TFT (TFT1), and a capacitor (C1) (see Figure 1; Column 5, Lines 53-65).

In regards to claim 7, Hamada et al. disclose another TFT (TFT2) (see Figure 1; Column 5, Lines 53-65).

In regards to claim 8, Hamada et al. disclose a common electrode (C2) connected to the capacitor (C1) and the TFT (TFT2) (see Figure 1; Column 5, Lines 53-65).

In regards to claim 9, Hamada et al. disclose a memory circuit (C1) (see Figure 1; Column 5, Lines 53-65).

In regards to claim 10, Hamada et al. disclose a liquid crystal display apparatus having a pair of substrates of which at least one substrate is transparent (see Column 6, Line 15) and a liquid crystal layer sandwiched between the substrates (see Column 1, Lines 20-21), comprising:

a plurality of first scanning electrodes formed on one of the substrates (see Figure 2 and Column 5, Line 55); and

a plurality of signal electrodes intersecting in a matrix form with the plurality of first scanning electrodes (see Figure 2 and Column 5, Line 54);

a plurality of second scanning electrodes provided along the first scanning electrodes or the signal electrodes (see Figure 5);

wherein the display apparatus further comprises, within each of the regions surrounded by the plurality of first scanning electrodes and the plurality of signal electrodes:

(a) a data holding circuit (TFT1 and C1) connected to a corresponding first scanning electrode, signal electrode, and second scanning electrode for fetching and storing display data from the signal electrode in response to voltages applied to the first and the second scanning electrodes (see Figure 5 and Column 6, Lines 54-55);

(b) a capacitor connected to the data holding circuit (see Figure 5 and Column 6, Lines 54-55);

(c) a switching device (TFT2) connected to the capacitor, its switching operation being controlled by a voltage of the capacitor (see Figure 5 and Column 6, Lines 59-65); and

(d) a display electrode (C2) connected to the switching device (see Figure 5 and Column 5, Lines 66-68).

In regards to claim 12, Hamada et al. disclose an opposed electrode (C'2) and a common electrode (C2) (see Figure 1; Column 5, Lines 53-65).

In regards to claim 13, Hamada et al. disclose connecting the display data holding circuit (TFT1 and C1) to the common electrode (C2) (see Figure 1; Column 5, Lines 53-65).

In regards to claim 14, Hamada et al. disclose a first TFT (TFT1) and a second TFT (TFT2).

In regards to claim 15, Hamada et al. disclose an LCD comprising: scanning electrodes (Y), signal electrodes (X), a TFT substrate with pixel circuits (C2), an opposed substrate (see Column 6, Line 15), a LC layer (see Column 1, Lines 20-21), switching control (Y), a first pixel circuit (C2), capacitive holding means (C1), pixel control means (TFT1), pixel driving TFT element (TFT2), a second pixel circuit (C'2), and a timing switch means (see Column 4, Lines 46-56).

In regards to claim 16, Hamada et al. disclose setting the second pixel circuit ON immediately before a rising or falling square wave voltage, and shifting LC form timings by about 180 degrees in phase (see Column 6, Lines 11-53).

In regards to claim 17, Hamada et al. disclose an n-channel and a p-channel TFT (see Column 6, Lines 11-53).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hamada et al. (5,194,974) in view of Yamaguchi et al. (5,627,557).

In regards to claims 3, 4 and 11, Hamada et al. disclose that the switching device for driving pixels is composed of a TFT device (see Figures 4 and 5): a signal for switching operation is input to a gate terminal of the TFT device, a drain terminal of the TFT device is connected to a display electrode, and a source terminal is connected to a reference line defining an average voltage of a liquid crystal drive voltage (see Column 4, Lines 9-13 and Column 8, Lines 33-38).

Hamada et al. do not disclose expressly including AC voltage generation means for generating a liquid crystal drive voltage nor timing signal generation means for generating a timing signal which is synchronized with a time when the liquid crystal drive voltage generated by the AC voltage generation means reaches an average voltage.

Yamaguchi et al. disclose including AC voltage (see Column 13, Lines 59-62) generation means for generating a liquid crystal drive voltage (see Figure 15 and Column 16, Lines 13-14) and timing signal generation means for generating a timing signal which is synchronized with a time when the liquid crystal drive voltage generated by the AC voltage generation means reaches an average voltage (see Figure 14 and Column 16, Lines 15-16).

Hamada et al. and Yamaguchi et al. are analogous art because they are from the shared field of liquid crystal displays utilizing capacitive charge storage. At the time of invention it would have been obvious to a person of ordinary skill in the art to use Yamaguchi's AC voltage generation means and timing signal generation means with Hamada's liquid crystal display. The motivation for doing so would have been to provide a means to create the scanning signals and data signals Hamada et al. already utilize in driving their liquid crystal display. Therefore it would have been obvious to combine Hamada et al. with Yamaguchi et al to obtain the invention as specified in claims 3, 4 and 11.

Conclusion

8. This is a continuation of applicant's earlier Application No. 08/820,835. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however,

event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (703) 305-8382. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6606 for regular communications and (703) 308-9051 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4700.

J.P.
March 23, 2001

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER